REMARKS

Claims 7-11, 13-17 and 19-29 are pending and at issue in the application with claims 7, 13 and 19 being independent claims. As a result, 3 independent claims remain in the application as previously paid for, and 21 total claims remain in the application as previously paid for. The applicants believe no additional fee is due. However, the Commissioner is hereby authorized to charge any deficiency in the amount enclosed or any additional fees which may be required under 37 CFR 1.16 or 1.17 to deposit account number 13- 2855. Reconsideration and withdrawal of the rejections in view of the remarks below is respectfully requested.

Claims 7, 8, 11, 19-21, 24-27 and 29 were rejected as anticipated under 35 U.S.C. §102(e) by Durcan et al. (U.S. Patent No. 6,395,600).[1] Claims 9, 10, 22, 23 and 28 were rejected as unpatentable under 35 U.S.C. §103(a) over Durcan et al., and claims 13-17 were rejected as unpatentable over Durcan et al. in view of Lee et al. (U.S. Patent No. 6,656,789). The applicant respectfully traverse these rejections.

Each of claims 7-11 recites a semiconductor device that includes capacitor plugs formed within a predetermined interval interleaved between two bit lines, lower electrodes of capacitors and contact pads formed between the lower electrodes and the capacitor plugs. The contact pads are disposed at a lower plane of at least one of the paired lower electrodes.

Each of claims 13-17 and 19-29 recites a method of fabricating a semiconductor device that includes forming a plurality of capacitor plugs within a predetermined interval interleaved between two bit lines and forming a plurality of lower electrodes of capacitors. Each of claims 19-29 further recites that contact pads are respectively formed between the lower electrodes and the capacitor plugs.

The applicants respectfully submit that claims 7, 8, 11, 19-21, 24-27 and 29 are not anticipated by Durcan et al. The action does not establish a *prima facie* case of anticipation,

[1] Although the text of the official action at the beginning of paragraph 2 on page 2 indicates that claims 14-16 are also rejected as anticipated by Durcan et al., the applicants believe this to be in error as there is no similar rejection of claim 13 from which claims 14-16 depend, and no reasons are provided for rejecting claims 14-16 as anticipated. On the other hand, the action does provide reasons in rejecting claims 14-16 as unpatentable over Durcan et al. in view of Lee et al.

because Durcan et al. fails to disclose all of the limitations of claims 7, 8, 11, 19-21, 24-27 and 29.

In particular, Durcan et al. fails to disclose capacitor plugs formed within a predetermined interval interleaved between two bit lines. Although Durcan et al. discloses method of forming a contact structure and a container capacitor structure that includes contact sites 5 filled with a conductive layer 24 and topped with a contact plug 69, the contact sites 5 (cited in the action as "capacitor plugs") are not formed between two bit lines. Instead, Durcan et al. discloses that bit line trenches are formed *over* the contact sites 5 and filled with a conductive layer 33 to form the contact plug 69. (See e.g., column 5, line 31 to column 6, line 14; Figs. 7-10). In other words, Durcan et al. discloses that capacitor plugs are formed *under* bit lines, and not between bit lines.

While the action cites "a bit line-to-bit line" (column 1, lines 38-47) and "adjacent bit lines" (column 8, lines 50-60), the citations read in their broader context merely refers to a memory array with a bit line-to-bit line pitch of 0.5 microns or less. Neither citation disclose the position of capacitor plugs as being between bit lines in any manner. Indeed, the citation of column 8, lines 50-60 actually states that the disclosed method of forming a contact structure and a container capacitor structure of Durcan et al. relates to formation of bit lines *over* the contacts. Although Durcan et al. also states that a buried bit line architecture may be used, this still does not disclose capacitor plugs formed *between* bit lines. Accordingly, Durcan et al. does not disclose capacitor plugs formed within a predetermined interval interleaved between two bit lines, as recited by claims 7, 8, 11, 19-21, 24-27 and 29.

Further, Durcan et al. fails to disclose contact pads formed between the lower electrodes and the capacitor plugs. As established above, Durcan et al. discloses contact plugs 69 formed over the contact sites 5.[2] Durcan et al. further discloses that the contact sites 5 are formed in a side-by-side horizontal arrangement to the conductive layer 20 forming the electrode (cited in the action as a lower electrode). (See e.g., Figs. 2A-12 and 14-22). As a result, it is impossible for a contact pad formed over the contact site 5 of Durcan et al. to be formed between contact site 50 and the electrode 20 based upon the side-by-side

[2] Element 1 cited in the action as a contact pad, actually refers only to the extent of the conductive layer's 24 encroachment towards contact sites 5. (See e.g., column 5, lines 24-26).

horizontal arrangement disclosed by Durcan et al. Accordingly, Durcan et al. cannot disclose ntact pads formed between the lower electrodes and the capacitor plugs, as cited by claims 7, 8, 11, 19-21, 24-27 and 29.

Regarding claims 7, 8 and 11, Durcan et al. fails to disclose that contact pads are disposed at a lower plane of at least one of the paired lower electrodes. As established above, the contact sites 5 of Durcan et al. are formed in a side-by-side horizontal arrangement to the conductive layer 20 forming the electrode. In addition, the contact plugs 69 formed over the contact sites 5. As a result, the contact plugs 69 are either on the same plane or on an upper plane of the electrodes. The contact plugs 69 of Durcan et al. are not disposed at a lower plane of at least one of a pair of electrodes, as recited by claims 7, 8 and 11.

It is clear that a claim is anticipated only if each and every element as set forth in the claim is found in a single prior art reference. *See* MPEP 2131. Accordingly, claims 7, 8, 11, 19-21, 24-27 and 29 are not anticipated by Durcan et al., because Durcan et al. does not teach or suggest all the limitations of claims 7, 8, 11, 19-21, 24-27 and 29, and the grounds for rejection of claims 7, 8, 11, 19-21, 24-27 and 29 as asserted in the action cannot be sustained.

The applicants respectfully submit that claims 9, 10, 22, 23 and 28 are not rendered obvious over Durcan et al. The action does not establish a *prima facie* case of obviousness, because Durcan et al. fails to disclose all of the limitations of claims 9, 10, 22, 23 and 28. As established above, Durcan et al. fails to disclose or suggest capacitor plugs formed within a predetermined interval interleaved between two bit lines, and contact pads formed between the lower electrodes and the capacitor plugs. Regarding claims 9 and 10, Durcan et al. further fails to disclose or suggest that contact pads are disposed at a lower plane of at least one of the paired lower electrodes.

It is clear that a claim cannot be rendered obvious where all the limitations of a claimed combination are not taught or suggested by the prior art. See *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). See also MPEP 2143.03. Accordingly, claims 9, 10, 22, 23 and 28 are not rendered obvious over Durcan et al., because Durcan et al. does not teach or suggest all the limitations of claims 9, 10, 22, 23 and 28, and the grounds for rejection of claims 9, 10, 22, 23 and 28 as asserted in the action cannot be sustained.

The applicants respectfully submit that claims 13-17 not rendered obvious over Durcan et al. in view of Lee et al. 35 U.S.C. §103(c) requires that subject matter developed by another person which qualifies as prior art under 35 U.S.C. §102(e) shall not preclude patentability under 35 U.S.C. §103 where the subject matter and the claimed invention where, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

In particular, Lee et al. and the instant application were commonly owned by Hynix Semiconductor Inc. at the time of the invention of the claimed subject matter. The assignment of the instant application to Hynix Semiconductor Inc. was recorded on September 27, 2004, and can be found at Reel 015186, Frame 0627. The assignment of Lee et al. was recorded on December 27, 2001, and can be found at Reel 012412, Frame 0954. Furthermore, Lee et al. is subject matter developed by another, which is only available as prior art under 35 U.S.C. §102(e), and has an issue date of December 2, 2003 after the applicants' filing date of July 23, 2003. A Statement of Common Ownership is filed simultaneously with the this paper. Accordingly, claims 13-17 cannot be rendered obvious over Durcan et al. in view of Lee et al, and the grounds for rejection of claims 13-17 as asserted in the action cannot be sustained.

For the foregoing reasons, reconsideration and withdrawal of the rejections of the claims and allowance thereof are respectfully requested. Should the examiner wish to discuss the foregoing, or any matter of form, in an effort to advance this application towards allowance, the examiner is urged to telephone the undersigned at the indicated number.

Respectfully submitted,

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